Amendments to the Specification:

Please amend paragraph 13 as indicated below.

[13]   Many other embodiments are possible. For instance, while the above description limits itself to logical processors, similar processing is applicable to physically separate multiprocessors that share any common execution resources. In such embodiments, a hybrid version of logical and physical multiprocessing is implemented where separate architectural states and some execution resources are separated in hardware, but other execution resources are shared in hardware and may be released using processing similar to that depicted in Fig. 2. In some embodiments, the thread scheduler referenced above may form a component of firmware resident in non-volatile memory as depicted in Fig. 3, while in others it may be a portion of operating system software stored on disk media accessible to the processor. In some embodiments, the actions taken to release and reserve processor execution resources may be directly implemented in hardware and ancillary to the processor's instruction execution system, while in other embodiments they may be actions taken by the processor as part of the execution of one or more instructions <u>of the processor's instruction set. That is, the instruction set may include one or more instructions which, when executed by a first logical processor, cause the first logical processor to make a processor execution resource previously reserved for the first processor available to a second processor</u>. In some embodiments the shared execution resources may include special purpose registers unrelated to the TLB. Embodiments are not limited to two processors, three or more processors may share execution resources and perform processing analogous to the processing described above.